

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	((("6578174") or ("7073158") or ("7024636")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/10/05 09:43
L2	6772	((703/28) or (716/106,107,108,136) or (714/11)).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/10/05 09:46
L3	116	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/10/05 10:52
L4	2078	((virtual emulat\$4 simulat\$5 test\$3) adj (processor) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/10/05 11:00
L5	2029	((virtual emulat\$4 simulat\$5 test\$3) adj (processor) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT	OR	ON	2011/10/05 11:02
L6	627	((virtual emulat\$4 test\$3) adj (cpu) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT	OR	ON	2011/10/05 11:49

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	109	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7))	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:06
L8	12	((virtual emulat\$4 simulat\$5 test\$3) adj (microcontroller) and (lock\$step\$3 synchroniz\$7)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:06
L9	36	((synchon\$7 lock\$step\$5) and (halt\$4 break\$4 stop\$4) and (cpu processor microprocessor microcontroller)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:09
L10	13	((synchon\$7 lock\$step\$5) same (halt\$4 break\$4 stop\$4) and (cpu processor microprocessor microcontroller)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:10
L11	10	((synchon\$7 lock\$step\$5) same (halt\$4 break\$4 stop\$4) same (cpu processor microprocessor microcontroller)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:36
L12	8	((synchon\$7 lock\$step\$5) and (halt\$4 break\$4 stop\$4) and (cpu processor microprocessor microcontroller) and (boot\$4 initial\$7)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:38

L13	0	((synchron\$7 lock\$step\$5) same (halt\$4 break\$4 stop\$4) same (cpu processor microprocessor microcontroller) same (boot\$4 initial\$7)).clm.	US- PGPUB; USPAT; UPAD	OR	ON	2011/10/05 12:39
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